Electronic Version
Stylesheet Version v1.1.1

[FLIP-CHIP PACKAGE SUBSTRATE AND FLIP-CHIP BONDING PROCESS THEREOF]

Abstract

The present invention provides a flip-chip package substrate including a plurality of stacked patterned circuit layers, a plurality of dielectric layers disposed between two neighboring patterned circuit layers and a plurality of bumps. The outmost layers of the patterned circuit layers include a plurality of first contacts and a plurality of second contacts. The bumps are connected to the corresponding first contacts. Since the bumps are formed on the substrate by low-cost implanting or printing apparatuses, the production cost of the flip chip package structure is lowered and the yield of the flip chip package process is improved.